IN THE CLAIMS

1. (Currently amended) A method of forming a gate in a non-volatile memory device comprising:

forming a tunnel dielectric layer on a semiconductor substrate;

forming a floating gate layer on the tunnel dielectric layer;

forming an intergate dielectric layer on the floating gate layer;

forming a control gate layer comprising an in-situ doped amorphous silicon layer on the intergate dielectric layer;

forming a metal silicide layer on the control gate layer;

[[thereafter,]]crystallizing the amorphous silicon layer by annealing the control gate layer after forming the metal silicide layer; and

patterning the control gate layer, the intergate dielectric layer, [[and]] the floating gate layer, and the metal silicide layer.

- 2. (Original) The method as claimed in claim 1, wherein forming a floating gate layer comprises forming polysilicon.
- 3. (Original) The method as claimed in claim 2, wherein forming a floating gate layer comprises forming amorphous silicon.
- 4. (Original) The method as claimed in claim 1, wherein the intergate dielectric layer comprises an oxide/nitride/oxide (ONO) film.
 - 5. (Cancelled)
 - 6. (Cancelled)
- 7. (Original) The method as claimed in claim 1, wherein annealing the control gate layer comprises furnace annealing.
- 8. (Original) The method as claimed in claim 7, wherein the furnace annealing is performed at a temperature of about 600~950°C.

- 9. (Original) The method as claimed in claim 1, wherein annealing the control gate layer comprises rapid thermal annealing (RTA).
- 10. (Original) The method as claimed in claim 9, wherein the RTA is performed at a temperature of about 800~1,000°C.
 - 11. (Cancelled)
 - 12. (Cancelled)
 - 13. (Cancelled)
 - 14. (Cancelled)
 - 15. (Cancelled)
 - 16. (Cancelled)
 - 17. (Cancelled)
 - 18. (Cancelled)
 - 19. (Cancelled)
 - 20. (Currently amended) A method of forming a gate in a non-volatile memory device, the method comprising:

forming a tunnel dielectric layer on a semiconductor substrate;

forming a [[first silicon]]floating gate layer on the tunnel dielectric layer;

forming an oxide-nitride-oxide (ONO) intergate dielectric layer on the [[first silicon]]floating gate layer;

forming a second silicon layer as a control gate layer on the ONO layer; forming a metal silicide layer on the second silicon layer;

reducing a thickness variation of the ONO layer and a bird's beak phenomenon at the interface between the ONO layer and the second silicon layer by annealing the resultant structure; and

sequentially patterning the metal silicide layer, the [[second silicon]]control gate layer, the ONO layer and the [[first silicon]]floating gate layer[[.]].

wherein the resultant structure is annealed after forming the metal silicide layer.

- 21. (Previously presented) The method of claim 20, wherein the annealing is performed in an ambient including an inert gas.
- 22. (Currently amended) The method of claim 20, wherein forming the [[a]] metal silicide layer comprises using dichlorosilane gas to form a tungsten silicide layer.
 - 23. (Cancelled)